What is claimed is:

1. A method for fabricating a semiconductor device using a salicide (self aligned silicide) process, comprising the steps of:

providing a material to be silicided at least on the surface of an area to be silicided;

performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region;

providing a supplemental silicon layer over the surface; and

performing a second RTA process to form a second-reacted silicide region.

2. A method according to claim 1, wherein

the material comprises cobalt (Co).

3. A method according to claim 1, wherein

the material comprises titanium (Ti).

4. A method according to claim 1, wherein

the supplemental silicon layer is of poly-silicon formed by CVD (Chemical Vapor Deposition) technique.

5. A method according to claim 1, wherein

the supplemental silicon layer is of a-Si (amorphousness silicon)

formed by sputtering technique.

6. A method according to claim 1, further comprising the step of:

selectively removing non-reacted silicon from the second-reacted silicide region after the second RTA process.

7. A method according to claim 1, further comprising the step of:

doping an impurity into the supplemental silicon layer before the second RTA process, wherein

the impurity is of the same type as active regions.

8. A method according to claim 7, wherein

the impurity is doped into one of N-channel region and P-channel region.

9. A method for fabricating a semiconductor device using a salicide (self aligned silicide) process, comprising the steps of:

providing a silicon substrate;

providing a BOX (Buried Oxide) layer in the silicon substrate;

providing a filed oxide layer and a SOI (Silicon on Insulator) layer on the BOX layer;

providing a gate oxide layer on the SOI layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the SOI layer to surround the poly-silicon gate layer and gate oxide layer;

providing a material to be silicided on the surface;

performing a first RTA (Rapid Thermal Annealing) process to form first-reacted silicide regions in the poly-silicon gate layer and source/drain active areas of the SOI layer;

removing non-reacted material from the first-reacted silicide regions;

providing a supplemental silicon layer over the entire surface;

performing a second RTA process so that the first-reacted silicide regions react again with the supplemental silicon layer to form second-reacted silicide regions; and

selectively removing non-reacted silicon from the second-reacted silicide regions.

10. A semiconductor device that is fabricated by a method comprising the steps of:

providing a material to be silicided at least on the surface of an area to be silicided;

performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region;

providing a supplemental silicon layer over the entire surface; and

performing a second RTA process to form a second-reacted silicide region.

11. A semiconductor device according to claim 10, wherein the silicide material comprises cobalt (Co).

12. A semiconductor device according to claim 10, wherein the silicide material comprises titanium (Ti).

13. A semiconductor device according to claim 10, wherein the supplemental silicon layer is of poly-silicon formed by CVD (Chemical Vapor Deposition) technique.

14. A semiconductor device according to claim 10, wherein the supplemental silicon layer is of a-Si (amorphousness silicon) formed by sputtering technique.

15. A semiconductor device according to claim 10, wherein non-reacted silicon is selectively removed from the second-reacted silicide region after the second RTA process.

16. A semiconductor device according to claim 10, wherein

an impurity is doped into the supplemental silicon layer before the second RTA process, and

the impurity is of the same type as active regions.

17. A semiconductor device according to claim 16, wherein

the impurity is doped into one of N-channel region and P-channel region.

18. A semiconductor device that is fabricated by a method comprising the steps of:

providing a silicon substrate;

providing a BOX (Buried Oxide) layer in the silicon substrate;

providing a filed oxide layer and a SOI (Silicon on Insulator) layer on the BOX layer;

providing a gate oxide layer on the SOI layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the SOI layer to surround the poly-silicon gate layer and gate oxide layer;

providing a material to be silicided on the surface;

performing a first RTA (Rapid Thermal Annealing) process to form first-reacted silicide regions in the poly-silicon gate layer and source/drain active areas of the SOI layer;

removing non-reacted material from the first-reacted silicide

regions;

providing a supplemental silicon layer over the entire surface;

performing a second RTA process so that the first-reacted silicide regions react again with the supplemental silicon layer to form second-reacted silicide regions; and

selectively removing non-reacted silicon from the second-reacted silicide regions.